High-Performance Three-Dimensional On-chip Inductors in SOI CMOS Technology for Monolithic RF Circuit Applications

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Abstract — **This paper presents high-Q and high-inductance-density on-chip inductors fabricated on high-resistivity substrate (HRS) using a 0.12 μm SOI CMOS technology with 8 copper metal layers. A peak Q of 52 is obtained at 5 GHz for a 0.6 nH STP (Single-turn, multiple metal levels in Parallel) inductor. An inductance density of 5302 fH/μm² is obtained for a 42 nH MTS (Multi-turn, multiple metal layers in Series) inductor.**

I. Introduction

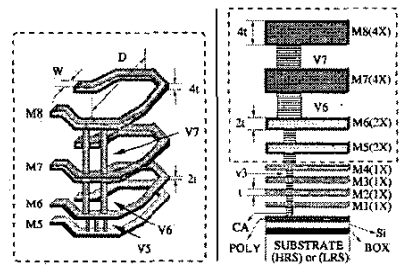
High-performance on-chip inductor is a key enabling element of monolithic RF circuits and RF system-on-chip (SOC) [1, 4]. The RF monolithic circuits such as VCOs, LNAs, mixers and PAs have different inductor specifications. For example, VCOs require very high Q and low inductance, LNAs and mixers require moderate Q and moderate inductance, and PAs require moderate Q and high inductance. To satisfy this wide range of inductor specifications simultaneously, we use three different types of the inductor geometry, high-resistivity SOI substrates, and thick copper metal layers [1]. The inductor geometries are denominated as STP, MTS and MTP (Multi-turn, multiple metal levels in Parallel). The STP inductors have the highest Q but consume the most chip area, the MTP inductor have moderate Q and are much more area efficient, and the MTS inductor achieves the highest inductances with the greatest inductance density and moderate Q [3, 4]. All these inductors are fabricated on LRS (Low resistivity substrate) (10~20 Ω·cm) and HRS (300 Ω·cm) for comparison using a 0.12 μm SOI CMOS technology with 8 copper metal layers.

II. On-chip Inductor Geometries

These three different inductor geometries use different metal stacking schemes to trade-off quality-factor Q and inductance density [3] [4] [6].

A. STP inductors

A diagram of an STP inductor, showing its single turn of multiple levels strapped together, is shown in Figure 1(a). This scheme improves metal conductance, with is further enhanced by the use of copper [3, 4, 6, 8]. We stacked up to 4 metals, M8 to M5, to obtain high Q. The vias V5-V7, serve as the contacts between metal layers, as shown in Figure 1(a).



(a) (b)

Fig. 1. (a) The STP inductor (b) Cross section of a 0.12 μm SOI CMOS technology

The thickness of levels M7 and M8 is 1.2 μm, the thickness of M5 and M6 is 0.6 μm, and the other metal levels are 0.3 μm thick.

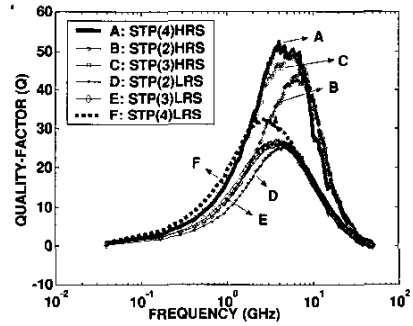


Fig. 2. Measured Q of the STP inductors (The number in parenthesis refers to the number of metal levels in parallel; "2" refers to M7 and M8, "3" to M6,M7 and M8, etc.)

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Figure 2 shows the measured quality-factor (Q) of the STP inductors. As the number of metal levels increases, the peak Q increases, but the self-resonant frequency (fo) decreases due to the increasing capacitance between the bottom metal layer and the substrate. HRS boosts inductor Q by at least 50 % by reducing substrate losses. The highest Q obtained is about 52 at 5 GHz with a 4-level STP inductor on HRS, with an inductance density of 6 fH/μm².

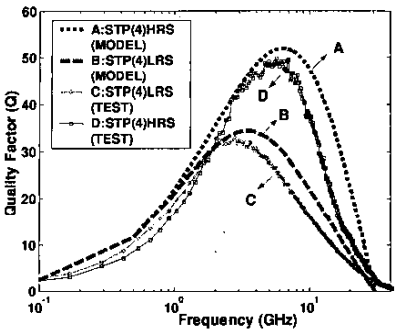


Fig. 3. Comparison Q: model value and test value (MODEL: simulation value and TEST: measured value)

Various inductor models have been developed to predict the characteristics of on-chip inductors [1, 4]. Figure 4 shows a diagram of the model we use, which is scalable in terms of substrate resistivity, number of turns, and number of metal levels stacked in parallel. Part III in Figure 4 does not apply to STP inductors due to the lack of inter-turn capacitance. Figure 3 shows the Q comparison between model and measurement. Model values are well matched with the measured data. The STP inductor can be used for RF circuits such as LC-tank oscillators that require high Q passives to satisfy low power and low phase noise requirements [2].

B. MTP inductors

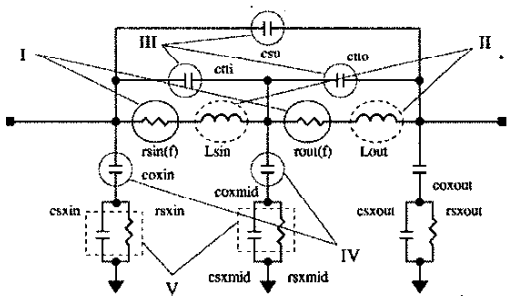


Fig. 4. A universal inductor model

The MTP inductor is similar to the STP inductor but it has more turns to increase the inductance value, as shown in Figure 11(b). This type is the most popular type of on-chip inductor, and its inductance density is much greater than that of STP inductors. However, its Q is less because of additional parasitic capacitance and narrow wire width [6]. The model in Figure 4 can be used for MTP inductors, with the capacitors of part III of the model representing inter-turn and turn-to-underpass capacitance [2, 3]. Part I represents the series resistance of inductor. This resistance is the resistance of the copper wires, and is frequency dependent due to the skin effect. Part II represents the inductance. Part IV represents capacitance between the lowest metal level and the substrate. Part V is a substrate model with a parallel RC circuit [5].

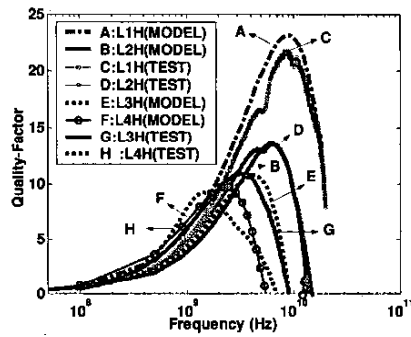


Fig. 5. Comparison Q: test value and model value
(Inductor 1 has 1.5 turns, inductor 2 has 2.5 turns, inductor 3 has 4.5 turns, and inductor 4 has 7.5 turns, All inductors are on HRS)

Figure 5 shows the comparison between modeled and measured values of Q with the number of inductor turns varied. The model fits well for all four inductors.

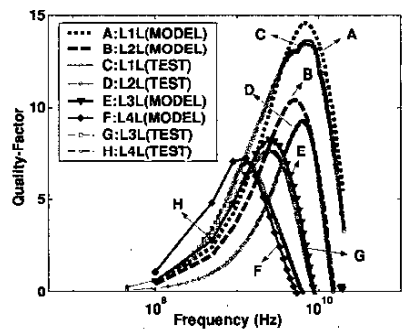


Fig. 6. Comparison Q: test value and model value
(Same inductors as in Figure 5, but on LRS)

Figure 6 is the same as Figure 5, except that the inductors are fabricated on LRS, and the model is changed accordingly. The model and measured data are just as well matched on LRS as on HRS. MTP inductors allow a trade-off between Q value and chip area. A small number of turns can be used for high Q while a higher number of turns can be used to save area. MTP inductors with optimized design can be used for both narrow band and wide band applications.

C. MTS inductors

Figure 7 shows the wiring scheme of MTS inductors. Multiple turns are made on each metal level, and these turns are connected in series to make the total turn number high while keeping the area low. The inductance tends to be high, though Q is moderately low [4, 6, 7].

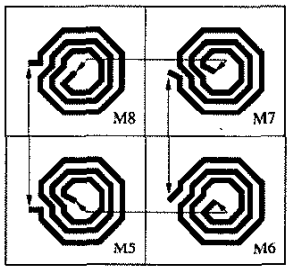


Fig. 7. MTS inductor diagram

Figure 11(c) shows the top view of the MTS inductor and a detailed metal connection is shown in Figure 7. The end of M8 is connected into the end of M7 and the front of M7 goes to the front of M6. The end of M6 is connected into the end of M5. Due to the series connection between levels, one terminal of this inductor is on M8 and the other is on M5. The total inductor length is four times longer than that of a similar MTP inductor.

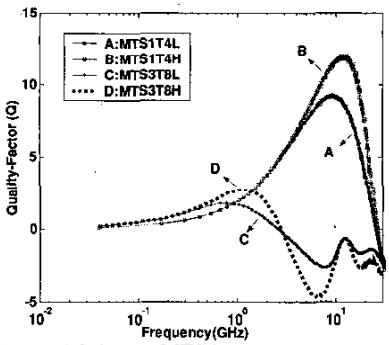


Fig. 8. Measured Q for the MTS inductors
("1T4" refer to 1 turn on each of 4 metal levels. "3T8" refers to 3 turns on each of metal levels. "L" is LRS, "H" is HRS).

Figure 8 shows the measured Q of two MTS inductors. For high inductance density, as many metal layers and turns as possible are used. The MTS3T8 inductor has very high inductance density but Q is relatively low, as shown in Figure 8. However, the MTS1T4 has improved Q and higher self-resonant frequency. Measured inductance values for these inductors are shown in Figure 9. The MTS3T8 inductor is 42 nH and the MTS1T4 inductor is 2 nH. These two inductors give approximate bounds on the inductance, Q and inductance density achievable with MTS inductors. Table 1 shows the inductance density of various inductors of different types. The MTS3T8 inductor has a density of 5302 fF/μm², which is about 900 times higher than the density of STP inductors. The MTS inductors can be applied as choke coils for RF amplifiers and the broad band application.

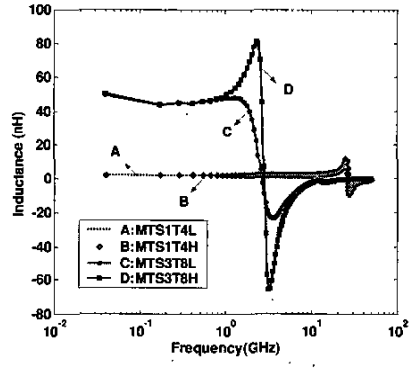


Fig. 9. Measured inductance for the MTS inductors
(Same inductors as in Figure 8)

TABLE I
COMPARISON Q AND INDUCTANCE DENSITY

INDUCTOR	(nH)	Peak-Q@GHz	Area(μm²)	(fH/μm²)
STP(4)H	0.6	52@5	90,000	6
MTP3.5T(2)H	2.5	21@3	67,600	36
MTS1T4H	2	12@8	7,921	252
MTS2.75T5L	17	7@2	19,600	867
MTS3T8H	42	2.5@1	7,921	5,302

(Here, H: HRS, L: LRS, (4): M8-M5 parallel stack, (2):M8-M7 parallel attack, 1T4:1-turn and M8-M5 series stack, 2.75T5: 2.75-turn and M8-M4 series stack, 3T8: 3-turn and M8-M1 series stack.)

III. DISCUSSIONS

On-chip inductor Q can be improved through use of HRS instead of LRS, as well as use of the appropriate metal stacking scheme [2, 8]. The substrate model is an R-C parallel circuit shown as in Part V of Figure 4 and the substrate effect can be reduced with the increase of substrate resistance. There is some variation of Q improvement due to inductor geometry in Table 2.

TABLE II
COMPARISON PEAK-Q

INDUCTOR	Q(LRS)	Q(HRS)	Δ(%)
STP(2)	24	45	87
STP(3)	25	49	82
STP(4)	32	52	62
MTS3T8	1.9	2.8	47
MTS1T4	9.2	12	30

For the STP inductors with the highest Q, use of HRS can improves Q by at least 50 %. Additionally, HRS enhances the signal isolation between circuits [5].

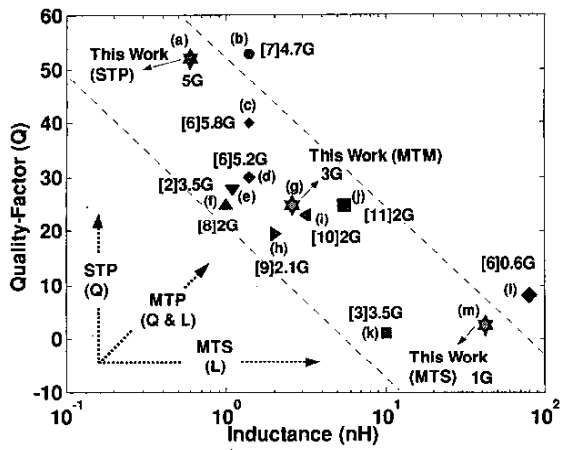
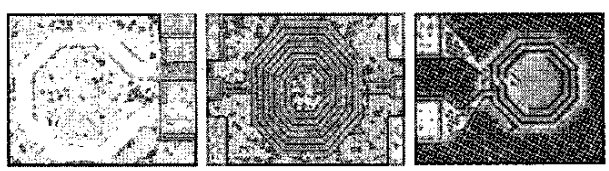


Fig. 10. Inductance versus Q
(The numbers near the symbols are the reference number and the frequency in GHz.)

There are two main regimes in the on-chip inductor design space: the high-Q regime and the high-inductance-density regime [6]. In Figure 10, we compare our work with data from publications [2]-[11] from groups that used a variety of fabrication techniques. Many of these techniques are non-standard, add substantial cost, or difficult to integrate with a typical CMOS process. All the inductors proposed inductors in this work are integrated with a standard digital CMOS technology (0.12-μm SOI CMOS) and do not require any extra masks. The marker (l, ref(6)) represents an 80 nH of inductance value but the inductance density is 320 fH/μm² while the MTS3T8 inductor (marker, m) has 5302 fH/μm². For high-Q regime, the marker (b, ref(7)) represents 52.8 of Q through a GaAs technology while the STP(4) (marker, a) has 52 of Q through a standard SOI CMOS technology. Figure 11 shows microphotographs of three different types of on-chip inductors. The top view of the STP(4) inductor is shown in Figure 11(a), the MTP7.5T2 in Figure 11(b) and the MTS3T8 in Figure 11(c).



(a) (b) (c)

Fig. 11. Microphotographs for on-chip inductors
((a). STP(4) inductor (b). MTP7.5T2 inductor (c). MTS3T8 inductor)

IV. Conclusion

Three different types of on-chip inductors in 0.12-μm SOI CMOS technology were discussed with optimum RF circuit applications. The best Q of on-chip inductors is obtained over 52 through the STP(4) inductor with HRS. The highest inductance density produced up to 5302 fH/μm² by the MTS3T8 inductor. To improve inductor Q is required of both STP geometry and HRS. The MTS geometry can boost dramatically inductance density.

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